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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In Re PATENT APPLICATION Of:

Applicant:	Chao-Cheng Lee	)
Serial No.:	10/748,667	)
Filed:	December 31, 2003	) AMENDMENT
For:	AMPLIFIER CIRCUIT	)
Attny Ref.:	TOP 348	)

August 19, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is in response to the Official Action mailed on May 19, 2005. No fee is due. However, please charge our Deposit Account No. 18-0002 if any fees are needed to enter this paper, and please advise us accordingly. It is noted that no petition is required because of the authorization to charge, but please consider this paper a petition for extension of time if needed.

The specification is amended colloquially to recite "inverting input" instead of "converting input".

I certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (fax no. 571-273-8300) on August 19, 2005.

Nick Bromer [reg. no. 33,478] *Signature* Nick Bromer

IN THE SPECIFICATION

The two paragraphs starting at page 3, line 24:

To achieve the above-mentioned object, the present invention provides an amplifier circuit having a high time constant. An operational amplifier includes a non-inverting ~~converting~~ input terminal coupled to a ground, a inverting ~~converting~~ input terminal and an output terminal. A first resistor network including at least one stage is coupled between the inverting ~~converting~~ input terminal and the input terminal. Each stage of the first resistor network includes a first node, a first current path and a second current path connected to the first node. The first current path of each stage of the first resistor network is connected to the first node of the next stage, the second current path of each stage of the first resistor network is grounded, and the first current path of the first stage of the first resistor network is connected to the inverting ~~converting~~ input terminal. A loading unit is coupled between the inverting ~~converting~~ input terminal and the output terminal.

In addition, the present invention provides another amplifier circuit having a high time constant. An operational amplifier includes a non-inverting ~~converting~~ input terminal coupled to a ground, a inverting ~~converting~~ input terminal and an output terminal. A resistor network including a plurality of stages is connected between the inverting ~~converting~~ input terminal and the output terminal. Each stage of the resistor network includes a node, a first current path and a second current path connected to the node. The first current path of each stage of the resistor network is connected to the node of the next stage of the resistor network, the second current path of each stage resistor network is grounded, and the first current path of the last stage of the resistor network is connected to the inverting ~~converting~~ input terminal. A loading unit is coupled to the inverting ~~converting~~ input terminal.

The paragraphs starting at page 6, line 23:

FIG. 6~Fig. 8 are the diagrams of the amplifier circuits according to the embodiments of the present invention. The amplifier circuit comprises an operational amplifier 40 having a grounded non-inverting ~~converting~~ input terminal, a inverting ~~converting~~ input terminal coupled to the input voltage via a first resistor unit, and an output terminal coupled to the inverting ~~converting~~ input terminal via a second resistor unit. In the embodiments of the present invention, the first resistor unit, the second resistor unit, or both can be implemented by the resistor network disclosed in the present invention, as shown in FIG. 6, FIG. 7, and FIG. 8 respectively. If the resistor network comprises n stages, the resistance of the equivalent resistor is $R_{eq} = 2^N \times R$.

FIG. 9 is a circuit showing the differentiator circuit according to the embodiment of the present invention, comprising an operational amplifier 40 having a grounded non-reverse input terminal, a inverting ~~converting~~ input terminal coupled to the input voltage via a capacitor C41, and an output terminal coupled to the inverting ~~converting~~ input terminal via a resistor unit. In the embodiment of the present invention, the resistor unit can be implemented by the resistor network disclosed in the present invention, as shown in FIG. 9. If the resistor network comprises n stages, the resistance of the equivalent resistor is $R_{eq} = 2^N \times R$.

FIG. 10 is a circuit showing the integrator circuit according to the embodiment of the present invention, comprising an operational amplifier 40 having a grounded non-reverse input terminal, a inverting ~~converting~~ input terminal coupled to the input voltage via a resistor unit, and an output terminal coupled to the inverting ~~converting~~ input terminal via a capacitor C42. In the embodiment of the present invention, the resistor unit can be implemented by the resistor network disclosed in the present invention, as shown in FIG. 10. If the resistor network comprises n stages, the resistance of the equivalent resistor is $R_{eq} = 2^N \times R$.

FIG. 11 is a circuit showing the low-pass filter circuit according to the embodiment of the present invention, comprising an operational amplifier 40 having a grounded non-reverse input

terminal, a inverting ~~converting~~ input terminal coupled to the input voltage via a resistor R43, and an output terminal coupled to the inverting ~~converting~~ input terminal via a capacitor C43 and a resistor unit connected in parallel. In the embodiment of the present invention, the resistor unit can be implemented by the resistor network disclosed in the present invention, as shown in FIG. 11. If the resistor network comprises n stages, the resistance of the equivalent resistor is $R_{eq} = 2^N \times R$.

FIG. 12 is a circuit showing the high-pass filter circuit according to the embodiment of the present invention, comprising an operational amplifier 40 having a grounded non-reverse input terminal, a inverting ~~converting~~ input terminal coupled to the input voltage via a resistor unit and a capacitor C44 connected serially, and an output terminal coupled to the inverting ~~converting~~ input terminal via a resistor R44. In the embodiment of the present invention, the resistor unit can be implemented by the resistor network disclosed in the present invention, as shown in FIG. 12. If the resistor network comprises n stages, the resistance of the equivalent resistor is $R_{eq} = 2^N \times R$. The amplifier circuit, the differentiator, the integrator, the high-pass filter and the low-pass filter according to the embodiments of the present invention use the resistor network as resistive loading, so the equivalent resistance of the resistive loading is $R \cdot 2^N$, wherein N represents the stage number of the resistor network. Using resistor network comprising 16 stages as an example, the unit resistance is 0.024 Meg. In addition, the total resistance is only 1.176 Meg. Compared with conventional resistors, the resistor network requires only 1/1353 the resistance of the conventional resistor. Thus, the amplification factors of the amplifiers according to the embodiments of the present invention are more flexible by using the resistor network as the resistive loading. In addition, the differentiator, the integrator, the high-pass filter and the low-pass filter according to the embodiments of the present invention achieve higher time constant using the resistor network as the resistive loading.

IN THE CLAIMS

The listing of claims will replace all prior versions, and listing, of claims in the application:

Claim 1 (currently amended): An amplifier circuit, comprising:an operational amplifier having a ~~non-converting~~ first input terminal coupled to a ~~ground~~ common node, a ~~converting~~ second input terminal, and an output terminal;

a capacitive device coupled between the second input terminal and an input voltage; and

a resistor network comprising a plurality of stages connected serially, coupled between the ~~converting~~ second input terminal and the output terminal, wherein each stage of the resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ~~ground~~ common node; and

a second resistor coupled between the input node and the output node.

Claim 2 (currently amended): The amplifier circuit as claimed in claim 1, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 3 (currently amended): The amplifier circuit as claimed in claim 2, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim 4 (currently amended): An amplifier circuit, comprising:

an operational amplifier having a ~~non-converting~~ first input terminal coupled to a ~~ground~~ common node, a ~~converting~~ second input terminal, and an output terminal;

a first resistor network comprising a plurality of stages connected serially, coupled to the ~~converting~~ second input terminal for receiving an input voltage, wherein each stage of the first resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ~~ground~~ common node; and

a second resistor coupled between the input node and the output node; and

a loading unit coupled between the ~~converting~~ second input terminal and the output terminal.

Claim 5 (currently amended): The amplifier circuit as claimed in claim 4, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 6 (currently amended): The amplifier circuit as claimed in claim 5, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim 7 (currently amended): The amplifier circuit as claimed in claim 4, wherein the loading unit is a second resistor network comprising a plurality of stages connected serially, wherein each stage of the first resistor network comprises an input node, an output node, a third

resistor coupled between the input node and the ~~ground~~ common node, and a fourth resistor coupled between the input node and the output node.

Claim 8 (currently amended): The amplifier circuit as claimed in claim 7, wherein the resistance of the third resistor is approximately two times larger than the resistance of the fourth resistor.

Claim 9 (currently amended): The amplifier circuit as claimed in claim 8, wherein the equivalent resistance of the resistor network is approximately $2n \times R$, wherein the resistor network includes n stages and the resistance of the fourth resistor is R.

Claim 10 (currently amended): ~~A resistor network includes a plurality of stages connected serially, wherein each stage of the first resistor network comprises:~~

~~an input node;~~

~~an output node;~~

~~a first resistor coupled between the input node and the ground; and~~

~~a second resistor coupled between the input node and the output node, wherein the resistor network is implemented inside of an IC device~~ The amplifier circuit as claimed in claim 4, wherein the loading unit comprises a capacitive device.

Claim 11 (currently amended): The amplifier circuit as claimed in claim ~~10~~ 4, wherein the ~~resistance of the first resistor is two times larger than the resistance of the second resistor~~ loading unit comprises a resistor device.

Claim 12 (currently amended): The amplifier circuit as claimed in claim 11, wherein the ~~equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R~~ resistor device comprises a second resistor network.

Claim 13 (currently amended): The amplifier circuit as claimed in claim ~~10~~ 4, ~~wherein each of the first resistor and the second resistor is implemented by a MOS transistor~~ further comprising a capacitive device coupled between the first resistor network and the input voltage.

Claim 14 (new): An amplifier circuit, comprising:

an operational amplifier having a first input terminal coupled to a common node, a second input terminal, and an output terminal;

a capacitive device coupled between the second input terminal and the output terminal; and

a resistor network comprising a plurality of stages connected serially, coupled between the second input terminal and the output terminal, wherein each stage of the resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the common node; and

a second resistor coupled between the input node and the output node.

Claim 15 (new): The amplifier circuit as claimed in claim 14, wherein the second input terminal is coupled to an input voltage.

Claim 16 (new): The amplifier circuit as claimed in claim 14, wherein the resistance of the first resistor is approximately two times larger than the resistance of the second resistor.

Claim 17 (new): The amplifier circuit as claimed in claim 16, wherein the equivalent resistance of the resistor network is approximately 2n×R, wherein the resistor network includes n stages and the resistance of the second resistor is R.

Claim 18 (new): The amplifier circuit as claimed in claim 14, further comprising a loading unit coupled between the second input terminal and an input voltage.

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REMARKS

Claims 1-13 have been amended. Claims 4-9 were allowed. Claims 10-13 are amended to all depend from allowed claim 4. New claims 14-18 are allowable for the reasons below.

Claim 1 has been amended by adding a capacitive device coupled between the second input terminal and an input voltage. Support for the amendment is shown in FIG. 9, wherein an inverting input terminal is coupled to an input voltage via a capacitor C_{41}.

Claim 1 and allowed Claims 4 and 7 have been amended by changing terminal names of the operational amplifier; no subject matter has been added. It is noted that this amendment of Claim 1, and the amendment of allowed Claims 4 and 8, is not for overcoming any rejection.

Claims 2-3 and allowed Claims 5-6 and 8-9 have been amended by adding the term "approximately." It is noted that this amendment of Claim 2-3 and allowed Claims 5-6 and 8-9 is for clarity, not for overcoming any rejection.

Claims 10-13 have been amended to depend from allowed Claim 4 and its related claims. Support for the amendment of Claim 10 is shown in FIG. 10, of Claim 11 in FIG. 6, of Claim 12 in FIG. 8, and of Claim 13 in FIG. 12. No new subject matter has been added.

35 U.S.C. 102(b). Claims 1-3, and 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Schlotterer et al. (U.S. 5,525,985). This rejection is respectfully traversed.

Claim 1 recites an amplifier circuit comprising an operational amplifier having a first input terminal coupled to a common node, a second input terminal, and an output terminal; *a capacitive device coupled between the second input terminal and an input voltage*; and a resistor network comprising a plurality of stages connected serially, coupled between the second input terminal and the output terminal, wherein each stage of the resistor network comprises an input node; an output node; a first resistor coupled between the input node and the common node; and a second resistor coupled between the input node and the output node.

However, Schlotterer does not teach or suggest *a capacitive device coupled between the second input terminal and an input voltage*. In FIG. 3 of Schlotterer, there is no capacitive device coupled to the second input terminal.

For this reason, *inter alia*, the Applicant believes that claim 1 is allowable over the cited reference, along with its dependent claims 2-3.

35 U.S.C. 103(a). Claims 2-3, and 11-13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Aswell (U.S. 6,703,682 B2). This rejection is respectfully traversed.

The Applicant believes that claims 2-3 are allowable by their dependency from claim 1, which is allowable due to the reasons stated above.

New Claims. The new claim 14 recites, in part, "a capacitive device coupled between the second input terminal and the output terminal". The Applicant believes that it is clear that these limitations are not taught by the cited references. For this reason, *inter alia*, the Applicant believes that claim 14 is allowable over the cited reference. Insofar as claims 15-18 depend from claim 14 and its related claims, they are also allowable.

Conclusion. The Applicant has made every effort to place the present application in condition for allowance. For the reasons above, the Applicant requests allowance of all the claims. The Applicant thanks the Examiner for his thorough review of the present application and his allowance of claims 4-9.

Respectfully submitted,

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Date

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